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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,585	01/18/2002	Takahiro Sato	YAMAP0797US	1116

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EXAMINER	
WILLIAMS, JEFFERY L	
ART UNIT	**PAPER NUMBER**
2137	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/051,585	**Applicant(s)** SATO ET AL.	
	Examiner Jeffery Williams	**Art Unit** 2137	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 21 April 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-11.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☒ Other: See Continuation Sheet.

EMMANUEL L. MOISE
SUPERVISORY PATENT EXAMINER

Continuation of 11. does NOT place the application in condition for allowance because: Regarding the amendments to claims 1 and 6, the examiner notes the change in the scope of claims 1 and 6 and their depending claims. Previously, neither claim 1 nor the depending claims recited a RAM for storing an "encrypted intermediate code". The examiner notes that the amended claim 1 is not equivalent in scope to the previously presented claims 1 and 2. Claim 6 and the depending claims have not previously recited a RAM for storing an "encrypted intermediate code"..

Continuation of 13. Other: Response to Arguments

Applicant's arguments filed 4/21/06 have been fully considered but they are not persuasive.

Applicant's argue primarily that:

(i). However, applicants respectfully submit that an execution section "capable of interpreting" as recited in claim 5 does represent a structural distinction versus the prior art. Namely, in order for the execution section to be capable of interpreting an intermediate code, the execution section must be configured (i.e., via hardware, software, firmware, or a combination thereof) in order to perform such function. Otherwise, it is not capable of interpreting an intermediate code.
The Examiner has not shown that Stokes is in any way configured or
programmed to carry out such function so as to be capable. Absent such showing,
applicants respectfully submit that the rejection of claims 5 and 6 is improper and
should be withdrawn for at Least such reason alone. (Remarks, pg. 2).

Regarding the above reason submitted by the applicant for traversal of the rejection of claims 5 and 6 under 35 U.S.C. 102(e), the examiner respectfully asserts that Stokes teaches the limitations as claimed.
First, the examiner points out that the claim limitation - an execution section for executing an interpreter program that is capable of interpreting an intermediate code, so as to generate a control command string (claim 5) - implies an interpreter that is capable of interpreting code so as to control the functionality of something. In response to applicant's argument that Stokes does not teach an interpreter program that is capable of interpreting an intermediate code, so as to generate a control command string, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. Regarding the prior art, Stokes discloses an execution section that is capable of interpreting intermediate code (Stokes, 6:42-45, 49-51).

Second, as pointed out in the prior office action, the examiner again asserts that Stokes teaches an interpreter program that is capable of interpreting an intermediate code, so as to generate a control command string (Stokes, col. 6, lines 14-17, 42-45, 49-57). As shown, Stokes discloses an execution section for an executed program that results in the commanding of the device to record/reproduce information in a controlled manner.

(ii) Accordingly, applicants respectfully submit that they are completely entitled to
refer to the teachings of Kittirutsunetorn to clarify that Stokes is not teaching what the
Examiner proposes.
That being said, the text in Stokes cited by the Examiner refers to a discussion of
prior art U& 5,081,675 to Kittirutsunetorn. The Examiner basically relies on Kittirutsunetorn as teaching the RAM, ROM and CPU on a single integrated circuit.

In response, the examiner points out that claims 1 - 4 and 7 - 11 were rejected under 35 U.S.C. 103(a) as being obvious over Stokes, "Magnetic Optical Encryption/Decryption Disk Drive Arrangement", U.S. Patent 6,473,861 B1. Thus, the examiner does not "basically relies on Kittirutsunetorn" as alleged by the applicants. As previously stated, the rejection relies on the teachings and interpretations of Stokes and what would have been obvious to one of ordinary skill in the art.

As disclosed by Stokes, prior art shows an arrangement to provide data encryption. Stokes' disclosure of prior art makes clear that an arrangement of data encrypting elements can be contained on a single piece of silicon, an integrated circuit chip. That is, a processing element for executing algorithms or processing data in accordance with an algorithm, and memory storing data and algorithms can be arranged within a single chip (Stokes, col. 1, lines 36-50). Furthermore, Stokes discloses an arrangement of encrypting data, wherein it is desirable for purposes of security to contain and arrange together the data encrypting elements. The contained arrangement is for the security of the processing element ("CPU") and memory (ROM & RAM) with data (Stokes, col. 8, lines 10-13; col. 2, lines 16-19; col. 3, lines 5-10). Thus, while Stokes does not disclose the circuit of the CPU, RAM, ROM as being attached to a single piece of silicon, Stokes does disclose that it is known in the art that the attaching of memory and processing elements to a single piece of silicon is feasible. It would have been obvious to one of ordinary skill in the art to employ the method of attaching encryption elements (processor and memory) to a single chip. This would have been obvious because one of ordinary skill in the art would have recognized from the teachings of Stokes that such a method is employed by those of ordinary skill in the art, and that such a method could be used to arrange encryption elements within a contained manner for a level of security.

(iii) However, upon close review of Fig. 2(b) and the disclosure in column 12, lines 46-57 of Kittirutsunetorn, the reference itself teaches that the CPU is not formed together with the RAM and ROM on a single integrated circuit chip. Rather, Kittirutsunetorn simply teaches that the PASD and RAMU may be integrally formed on the same chip. The CPU is separate and apart from the package 119 including the RAMU and the PASD.

In response, the examiner makes note that the applicants' representative argues that the claimed CPU ("processing element" within the LSI device) of claim 5 is equivalent to the system CPU of Kittirutsunetorn (Kittirutsunetorn, 11:9-11). The examiner can find no support within the applicants' disclosure for such reasoning. Again, while the examiner points out that the teachings of Kittirutsunetorn have not been relied upon, the examiner respectfully directs that attention of the applicant's representative to the reference of Kittirutsunetorn. Kittirutsunetorn discloses that the processing elements and the memory of the device are contained within an integrated chip so as to hide information from the system CPU (Kittirutsunetorn, 19:30-61).